REMARKS

Claims 1-23 are pending. Claims 1-5, 7-10, 12, 14, 16, 18, and 20-23 are amended with this response. Please note that the amendments have been made to address highlighted issues associated with indefiniteness, and do not alter the scope of the claims. Because the amendments render the claims definite without raising new substantive issues, entry of the amendment after the final rejection is believed to be proper for reducing the number of outstanding issues. Reconsideration of the application is respectfully requested for at least the following reasons.

I. REJECTION OF CLAIMS 1-23 UNDER 35 U.S.C. § 112

Claims 1-23 were rejected under 35 U.S.C. § 112 second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The office action specifically states that, "[d]escription of the entry, the data frames, the receive descriptor ring, the descriptor management system and the counters are vague and indefinite."

Claims 1, 3, 5, 7 and 10 have been amended to address these issues. Claim 1 now specifies that entries indicate a number of incoming data buffers from which the host or driver can read incoming data. This amendment is supported by in the specification at pg. 9, lns. 9-13. Claim 3 has been amended to specify that each receive descriptor ring stores at least one of the one or more data descriptors indicating locations of incoming data buffers. This amendment is supported in the specification at pg. 12, lns. 9-12. Claim 5 has been amended to specify that the individual counters are used to determine whether the data stored in an associated transmit descriptor is ready to be transferred. This amendment is supported by the method shown in Fig. 1F and described in the specification between pg. 17, ln. 7 and pg. 19, ln. 23. Claim 7 has been amended to specify that each transmit descriptor ring stores at least one of the one or more data descriptors indicating locations of outgoing data buffers in the shared memory. This amendment is supported in the specification at pg. 12, lns. 7-9. Claim 10 has been amended in a similar manner with the above mentioned claim amendments.

Accordingly, withdrawal of the rejection for these claims and dependent claims is respectfully requested.

II. REJECTION OF CLAIMS 1, 2, AND 11 UNDER 35 U.S.C. § 102(b)

Independent claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,724,358 (Headrick et al.). Withdrawal of the rejection is respectfully requested for at least the following reason.

As amended, claim 1 of the present invention relates to a method of transferring data between a host and a network that comprises providing a data transfer queue in a shared memory comprising a priority level, one or more descriptors indicating a memory buffer location within the shared memory, and one or more entries indicating a number of memory buffers located within the shared memory from which the host can read or write the data. A part of the data, to be transferred from the host to the network, is retrieved from a memory buffer location indicated by the one or more descriptors. A part of the data, transferred from the network to the host, is stored in a memory buffer location indicated by the one or more descriptors. The amendments made to claim 1 in support of the above mentioned changes are supported by pg. 3, lns. 27-28 and the methods shown in Fig. 1C (described in the specification at pg. 13, lns. 19-27) and Fig. 1D (described in the specification at pg. 14, lns. 11- 23).

As will be argued below, Headrick et al. do not anticipate the present invention because Headrick et al. teach pointers stored in pointer memory pointing to ***data located in queues***, while the present invention claims data transfer queues comprising descriptors associated with ***data not located in the queues***.

In the abstract, Headrick et al. teach "pointers to buffer locations containing data packets having a particular priority level stored in one or more priority sub-queues" (abstract, line 9-11). The specification further explains what this means. The node 22 receives the data and the routing and buffering unit 126 stores the data with an internal tag (col. 6, line 1-2). For outputting data, data stored in the routing and buffering unit 126 is ***mapped directly to each output queue element*** (col. 9, line 47-49) contained

in the pointer memory 178,180 (col. 8, line 65). Each data entry further has a next memory location field 294. The output queue has a pointer memory associated with it (col. 9, line 49-50) which points with a head pointer to a memory location within the output queue. That memory location will be transferred and will also point to the location of the next memory location field. This process will repeat until the tail pointer is reached, at which time the pointer memory will advance to the next head pointer/priority level of the pointer memory (fig. 11). In this manner data is transferred from it's mapped to location in the queues located in the buffer memory.

This is different than claim 1 of the present invention, wherein the data queues comprise one or more descriptors indicating a memory buffer location within the shared memory, and one or more entries indicating a number of memory buffers located within the shared memory from which the host can read or write the data. Data to be transferred to the network ***is retrieved from a memory buffer location indicated by the one or more descriptors, which are stored in the plurality of data transfer queues.*** Data received from the network ***is stored in the memory buffer location indicated by the one or more descriptor, which are stored in the plurality of data transfer queues***. In contrast to Headrick et al., ***the queue of the present invention points to data stored separate from the queue. There is no mapping of data from the buffer memory to the queue***. Therefore, there is no need for pointer memory outside of the queue as required in Headrick et al. Since Headrick et al. fail to teach receive descriptors located in the data queues pointing to data stored outside the queue they fail to anticipate claim 1 of the present invention.

Independent claim 1 was rejected as being anticipated by Headrick et al. Claims 2 and 11 depend upon claim 1, respectively, and add further limitations thereto. The primary reference does not teach or suggest the present inventions of claim 1. Therefore claims 2 and 11 are also not anticipated by the cited art. Accordingly, withdrawal of the rejection is respectfully requested.

III. REJECTION OF CLAIMS 12, 13, 20, AND 21 UNDER 35 U.S.C. § 102(b)

Independent claims 12 and 20 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,724,358 (Headrick et al.). Withdrawal of the rejection is respectfully requested for at least the following reasons.

Claim 12 of the present invention relates to a system for transferring data between a host and a network using a shared memory comprising a plurality of data transfer queues comprising one or more descriptors indicating a memory buffer location storing the data to be transferred between the host and the network and a network interface system comprising a descriptor management system storing a plurality of priority levels, the priority levels being individually associated with one of the data transfer queues.

Claim 20 of the present invention relates to a network interface system comprising a descriptor management system storing a plurality of priority levels, the priority levels being individually associated with a data transfer queue in a shared memory, and wherein the network interface system transfers data between a buffer memory located within the host and the network

As stated above, Headrick et al. fail to teach one or more receive descriptors in a receive descriptor ring comprising the data transfer queues pointing to the data stored in a memory buffer outside the queue.

Further, in figure 1, Headrick et al. show a block diagram of an asynchronous transfer mode (ATM) communication system. The ATM communication system comprises a number of nodes 22 interconnected by communication links 42. Headrick et al. state that a node may include a plurality of input modules 80, a switch fabric 82 and a plurality of output modules (col. 4, line 20-21). Figure 5 shows a switch fabric 82 in more detail. The switch fabric of figure 5 comprises a router and buffering unit 126, a buffer manager 128, an input layer 122 and input translation 124, and an output layer 132 and output translation 134. Figure 7 shows the router and buffering unit 126 and buffer manager 128 in more detail. The buffer manager comprises pointer memory 178 and 180. Headrick et al. teach that output queues are stored in the pointer memories

178, 180 and further that sub-queues may be present ***within*** the overall output queue (*i.e.,* sub-queues are stored in the pointer memories also) (col. 9, line 56-58).

The network interface periphery as claimed in claims 1, 12, and 20 of the present invention comprises a descriptor management system storing a plurality of priority levels, the priority levels being individually associated with one of the data transfer queues. Headrick et al. teach that a combination of the output queue and the pointer memory determine the priority level and that sub-queues are used for multiple priority levels (col. 9, line 50-58). Queues, sub-queues are stored in pointer memories 178, 180 located in the buffer manager 128 (col. 8, line 61-65, col. 9, line 56-58). Headrick et al. do not teach any other storage of queues or sub-queues. Therefore***, for Headrick et al. to teach a network interface periphery it must comprise the buffer manager 128*** since it is necessary that it include the pointer memories 178, 180 which store the queues and sub-queues as taught by claims 1, 12, and 20.

The shared memory of claims 1, 12, and 20 of the present invention comprises data transfer queues. As previously stated, Headrick et al. teach that the pointer memories 178, 180 contain a plurality of linked list type data structures that ***are the output queues*** for the plurality of output ports. Therefore, for Headrick et al. to teach a shared memory comprising data transfer queues ***it is necessary that the shared memory also comprise the buffer manager 128*** (which comprises the pointer memories 178,180 which comprises the queues).

For Headrick et al. to anticipate the present invention: (1) the structure analogous to the network interface must consist of the buffer manager 128 so that the network interface contains a plurality of priority levels; and (2) the structure analogous to the shared memory must consist of the buffer manager 128 so that the shared memory contains the data queues. ***Since the shared memory and the network interface periphery are separate objects it is not possible that both comprise the buffer manager 128 as would be necessary for Headrick et al. to anticipate the present invention.*** Therefore, Headrick et al. do not anticipate the shared memory

and network interface periphery as taught in claims 1, 12, and 20 of the present invention.

Independent claims 12 and 20 were rejected as being anticipated by Headrick et al. Claim 13 depends upon claim 12 and adds further limitations thereto. Claim 21 depends upon claim 20 and adds further limitations thereto. The primary reference does not teach or suggest the present inventions of claims 12 or 20. Therefore claims 13 and 21 are also not anticipated by the cited art. Accordingly, withdrawal of the rejection is respectfully requested.

IV. REJECTION OF CLAIMS 3, 14, 22, AND 15 UNDER 35 U.S.C. § 103(a)

Claims 3, 14, 15, and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,724,358 (Headrick et al.). Withdrawal of the rejection is respectfully requested for at least the following reasons.

As stated above, Headrick et al. do not teach or suggest the invention of independent claims 1, 12, or 20. Claim 3 depends upon claim 1, and adds further limitations thereto. Claim 14 and 15 depend upon claim 12 and add further limitations thereto. Claim 22 depends upon claim 20 and adds further limitations thereto. Because the primary references do not teach the present invention of claims 1, 12, or 20, claims 3, 14, 15, and 22 are also non-obvious over the cited art. Accordingly, withdrawal of the rejection is respectfully requested.

V. CONCLUSION

For at least the above reasons, the claims currently under consideration are believed to be in condition for allowance.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 50-1733, AMDP762US.

Respectfully submitted,
ESCHWEILER & ASSOCIATES, LLC

By /Thomas G. Eschweiler/
Thomas G. Eschweiler
Reg. No. 36,981

National City Bank Building
629 Euclid Avenue, Suite 1000
Cleveland, Ohio 44114
(216) 502-0600